## The RF Sub–Micron MOSFET Line

# RF Power Field Effect Transistors

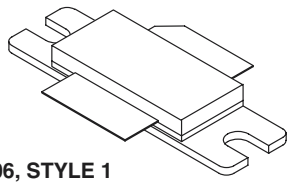
## N–Channel Enhancement–Mode Lateral MOSFETs

**MRF9135L**
**MRF9135LR3**
**MRF9135LSR3**

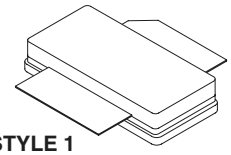
**880 MHz, 135 W, 26 V**
**LATERAL N–CHANNEL**
**RF POWER MOSFETs**

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 26 volt base station equipment.

- Typical N–CDMA Performance @ 880 MHz, 26 Volts, $I_{DQ}$ = 1100 mA
  IS–95 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  Output Power — 25 Watts Avg.
  Power Gain — 17.8 dB
  Efficiency — 25%
  Adjacent Channel Power —
  750 kHz: –47 dBc @ 30 kHz BW
- Internally Matched, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 135 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ″ Nominal.



**CASE 465–06, STYLE 1**
**NI–780**
**MRF9135L**



**CASE 465A–06, STYLE 1**
**NI–780S**
**MRF9135LSR3**

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 65 | Vdc |
| Gate–Source Voltage | $V_{GS}$ | +15, –0.5 | Vdc |
| Total Device Dissipation @ $T_C$ > = 25°C<br>Derate above 25°C | $P_D$ | 298<br>1.7 | Watts<br>W/°C |
| Storage Temperature Range | $T_{stg}$ | –65 to +200 | °C |
| Operating Junction Temperature | $T_J$ | 200 | °C |

### ESD PROTECTION CHARACTERISTICS

| Test Conditions | Class |
|---|---|
| Human Body Model | 1 (Minimum) |
| Machine Model | M2 (Minimum) |
| Charge Device Model | C7 (Minimum) |

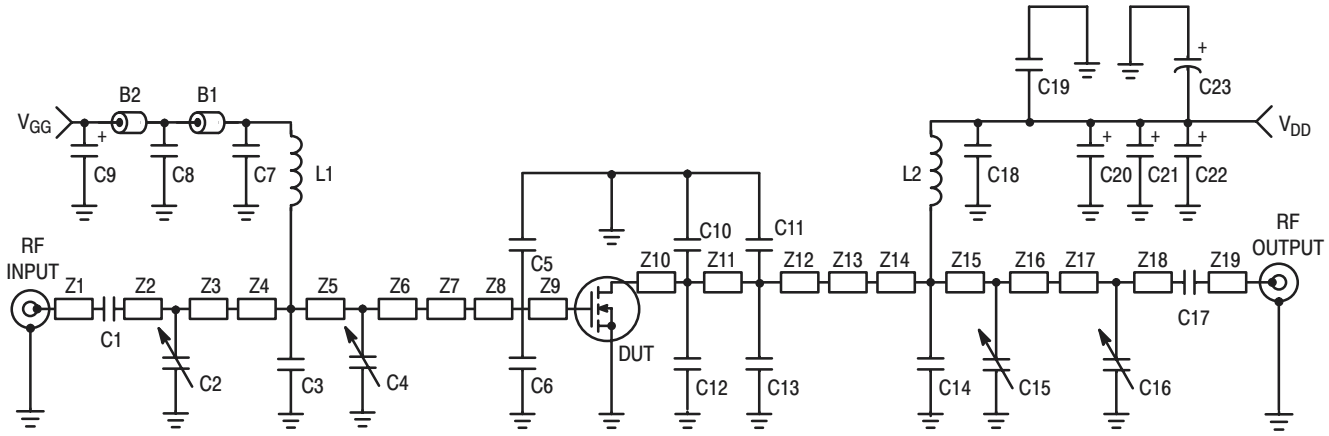
### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 0.6 | °C/W |

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C, 50 ohm system unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 65 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 10 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS}$ = 26 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 1 | μAdc |
| Gate–Source Leakage Current ($V_{GS}$ = 5 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | — | — | 1 | μAdc |
| **ON CHARACTERISTICS** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 10 Vdc, $I_D$ = 450 μA) | $V_{GS(th)}$ | 2 | 2.8 | 4 | Vdc |
| Gate Quiescent Voltage ($V_{DS}$ = 26 Vdc, $I_D$ = 1100 mAdc) | $V_{GS(Q)}$ | 3 | 3.7 | 5 | Vdc |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 3 Adc) | $V_{DS(on)}$ | — | 0.19 | 0.4 | Vdc |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 9 Adc) | $g_{fs}$ | — | 12 | — | S |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Output Capacitance ($V_{DS}$ = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, $V_{GS}$ = 0 Vdc) | $C_{oss}$ | — | 109 | — | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, $V_{GS}$ = 0 Vdc) | $C_{rss}$ | — | 4.4 | — | pF |
| **FUNCTIONAL TESTS** (In Motorola Test Fixture) Single–Carrier N–CDMA, 1.2288 MHz Channel Bandwidth Carrier, Peak/Avg. Ratio = 9.8 dB @ 0.01% Probability on CCDF | | | | | |
| Common–Source Amplifier Power Gain ($V_{DD}$ = 26 Vdc, $P_{out}$ = 25 W Avg. N–CDMA, $I_{DQ}$ = 1100 mA, f = 880.0 MHz) | $G_{ps}$ | 16 | 17.8 | — | dB |
| Drain Efficiency ($V_{DD}$ = 26 Vdc, $P_{out}$ = 25 W Avg. N–CDMA, $I_{DQ}$ = 1100 mA, f = 880.0 MHz) | η | 22 | 25 | — | % |
| Adjacent Channel Power Ratio ($V_{DD}$ = 26 Vdc, $P_{out}$ = 25 W Avg. N–CDMA, $I_{DQ}$ = 1100 mA, f = 880.0 MHz; ACPR @ 25 W, 1.23 MHz Bandwidth, 750 kHz Channel Spacing) | ACPR | — | –47 | –45 | dBc |
| Input Return Loss ($V_{DD}$ = 26 Vdc, $P_{out}$ = 25 W Avg. N–CDMA, $I_{DQ}$ = 1100 mA, f = 880.0 MHz) | IRL | — | –13.5 | –9 | dB |
| Common–Source Amplifier Power Gain ($V_{DD}$ = 26 Vdc, $P_{out}$ = 25 W Avg. N–CDMA, $I_{DQ}$ = 1100 mA, f = 865 MHz and 895 MHz) | $G_{ps}$ | — | 17 | — | dB |
| Drain Efficiency ($V_{DD}$ = 26 Vdc, $P_{out}$ = 25 W Avg. N–CDMA, $I_{DQ}$ = 1100 mA, f = 865 MHz and 895 MHz) | η | — | 24 | — | % |
| Adjacent Channel Power Ratio ($V_{DD}$ = 26 Vdc, $P_{out}$ = 25 W Avg. N–CDMA, $I_{DQ}$ = 1100 mA, f = 865 MHz and 895 MHz; ACPR @ 25 W, 1.23 MHz Bandwidth, 750 kHz Channel Spacing) | ACPR | — | –46 | — | dBc |
| Input Return Loss ($V_{DD}$ = 26 Vdc, $P_{out}$ = 25 W Avg. N–CDMA, $I_{DQ}$ = 1100 mA, f = 865 MHz and 895 MHz) | IRL | — | –12.5 | — | dB |
| Output Mismatch Stress ($V_{DD}$ = 26 Vdc, $P_{out}$ = 135 W CW, $I_{DQ}$ = 1100 mA, f = 880.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests) | Ψ | No Degradation In Output Power | | | |




| | | | |
|---|---|---|---|
| Z1 | 0.430″ x 0.080″ Microstrip | Z11 | 0.105″ x 0.630″ Microstrip |
| Z2 | 0.430″ x 0.080″ Microstrip | Z12 | 0.145″ x 0.630″ Microstrip |
| Z3 | 0.800″ x 0.080″ Microstrip | Z13 | 0.200″ x 0.630″ x 0.220″ Taper |
| Z4 | 0.200″ x 0.220″ Microstrip | Z14 | 0.180″ x 0.220″ Microstrip |
| Z5 | 0.110″ x 0.220″ Microstrip | Z15 | 0.110″ x 0.220″ Microstrip |
| Z6 | 0.175″ x 0.220″ Microstrip | Z16 | 0.200″ x 0.220″ Microstrip |
| Z7 | 0.200″ x 0.220″ x 0.630″ Taper | Z17 | 0.900″ x 0.080″ Microstrip |
| Z8 | 0.250″ x 0.630″ Microstrip | Z18 | 0.360″ x 0.080″ Microstrip |
| Z9 | 0.050″ x 0.630″ Microstrip | Z19 | 0.410″ x 0.080″ Microstrip |
| Z10 | 0.050″ x 0.630″ Microstrip | | |

**Figure 1. 880 MHz Test Circuit Schematic**

**Table 1. 880 MHz Test Circuit Component Designations and Values**

| Part | Description | Value, P/N or DWG | Manufacturer |
|---|---|---|---|
| B1, B2 | Short Ferrite Beads, Surface Mount | 95F786 | Newark |
| C1, C7, C17, C18 | 47 pF Chip Capacitors, B Case | 100B470JP 500X | ATC |
| C2, C16 | 0.6–4.5 Gigatrim Variable Capacitors | 44F3360 | Newark |
| C3 | 8.2 pF Chip Capacitor, B Case | 100B8R2BP 500X | ATC |
| C4, C15 | 0.8–8.0 Gigatrim Variable Capacitors | 44F3360 | Newark |
| C5, C6 | 12 pF Chip Capacitors, B Case | 100B120JP 500X | ATC |
| C8 | 20K pF Chip Capacitor, B Case | 200B203MP50X | ATC |
| C9, C20, C21, C22 | 10 μF, 35 V Tantulum Capacitors | 93F2975 | Newark |
| C10, C11, C12, C13 | 7.5 pF Chip Capacitors, B Case | 100B7R5JP 500X | ATC |
| C14 | 11 pF Chip Capacitor, B Case | 100B110JP 500X | ATC |
| C19 | 0.56 μF, 50 V Chip Capacitor | C1825C564K5RA7800 | Kemet |
| C23 | 470 μF Electrolytic Capacitor | 14F185 | Newark |
| L1, L2 | 12.5 nH Coilcraft inductors | A04T–5 | Coilcraft |
| WB1, WB2 | 10 mil Brass Shim (0.205 x 0.530) | RF–Design Lab | RF–Design Lab |
| PCB | Etched Circuit Board | 900 MHz 4X6 Cobra Rev 02 | CMR |
| Bedstead | Circuit Bedstead | DWG #990528JAM2 | RF–Design Lab |
| Board Material | 30 mil Glass Teflon®, $\varepsilon_r$ = 2.55, 2 oz Cu | GX–0300–55–22 | Arlon |

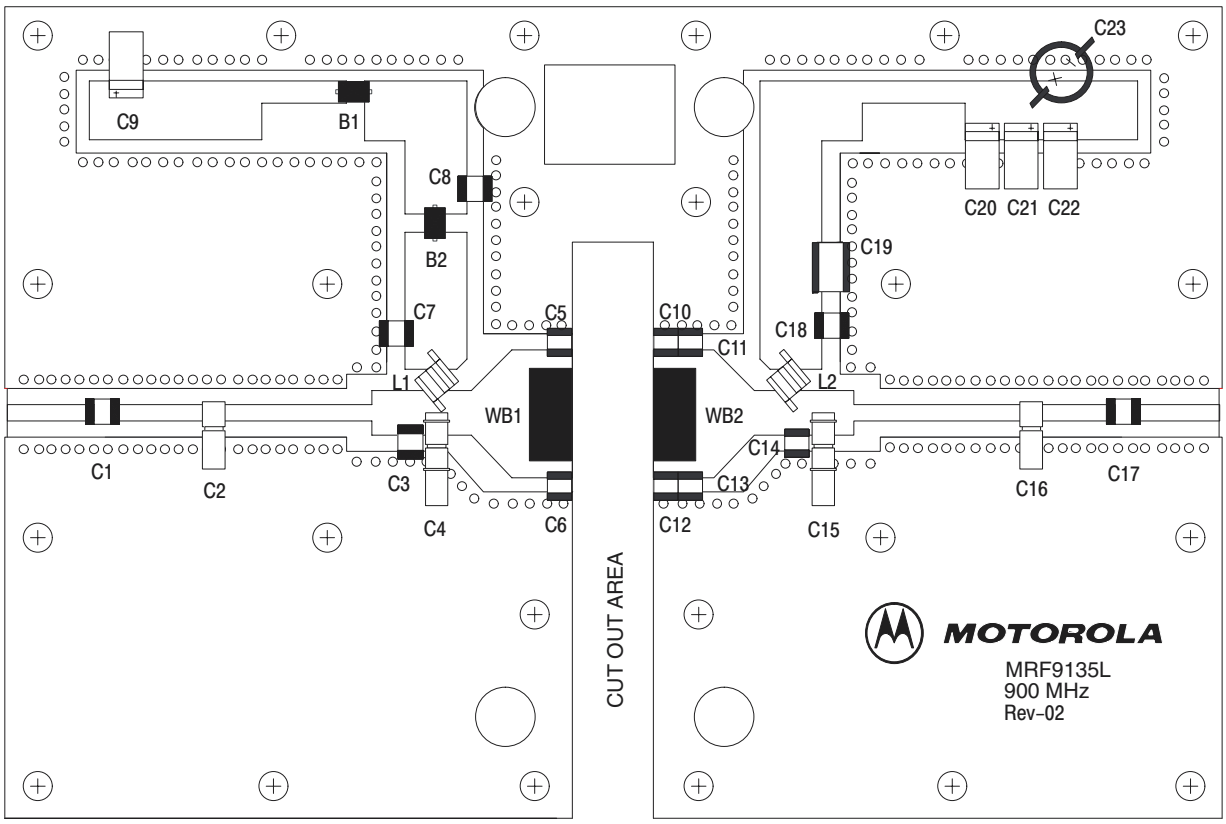



**Figure 2. 880 MHz Test Circuit Component Layout**

## TYPICAL CHARACTERISTICS

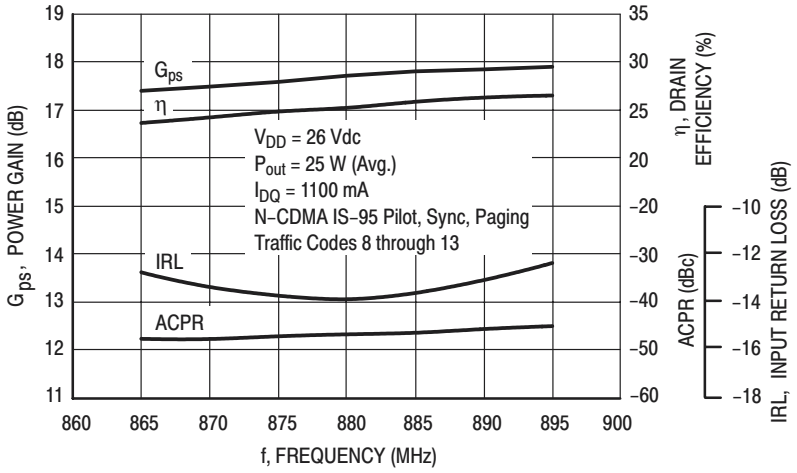



**Figure 3. Class AB Broadband Circuit Performance**

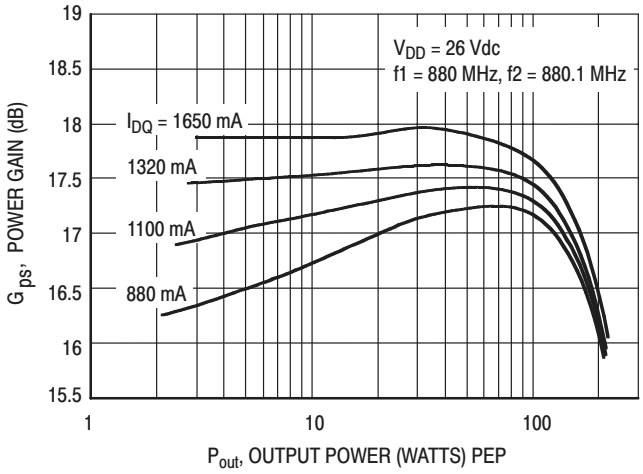



**Figure 4. Power Gain versus Output Power**

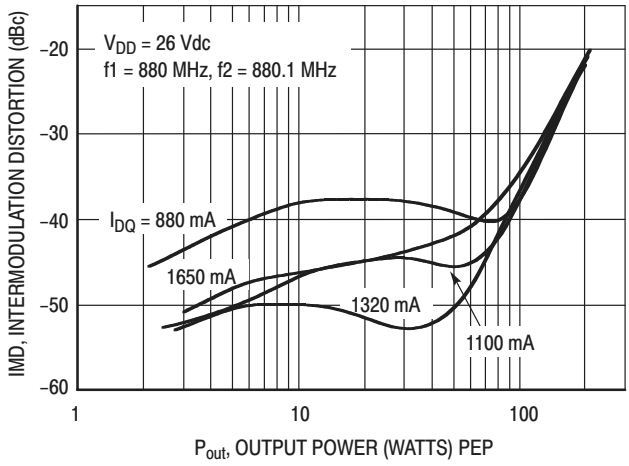



**Figure 5. Intermodulation Distortion versus Output Power**

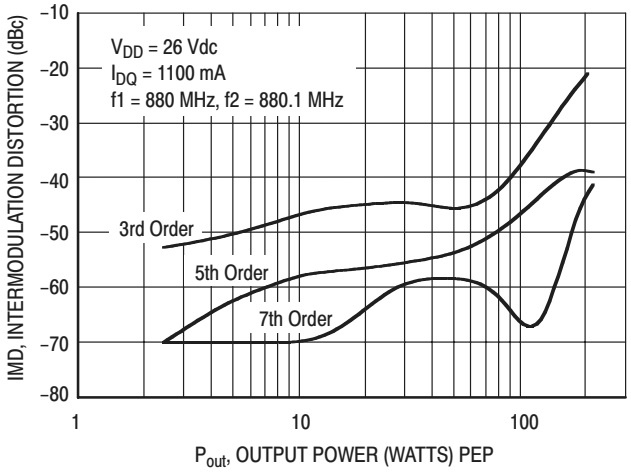



**Figure 6. Intermodulation Distortion Products versus Output Power**

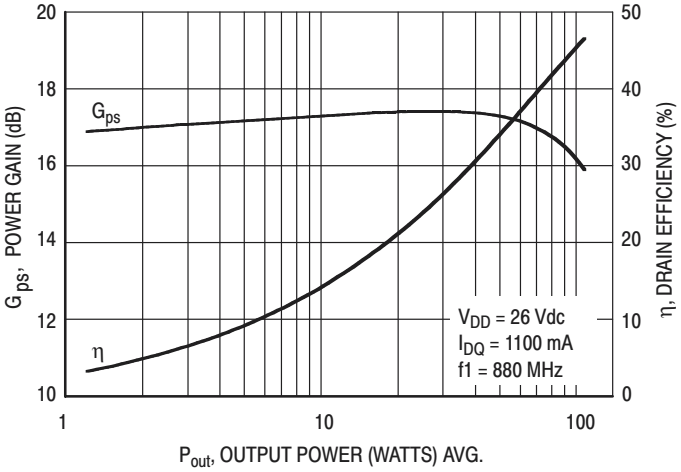



**Figure 7. Power Gain and Efficiency versus Output Power**

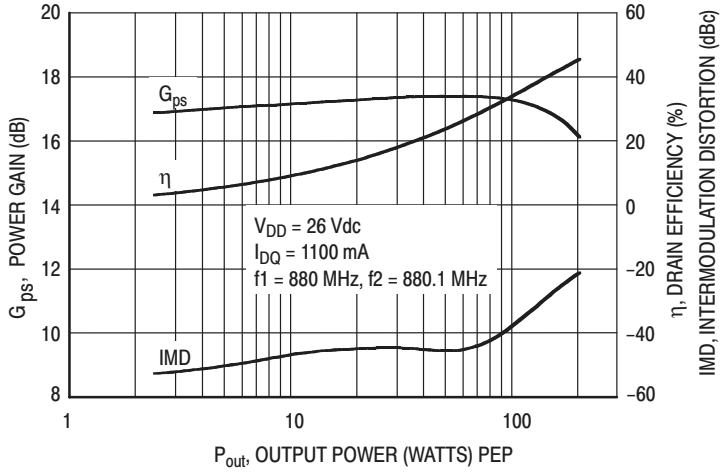



**Figure 8. Power Gain, Efficiency and IMD versus Output Power**

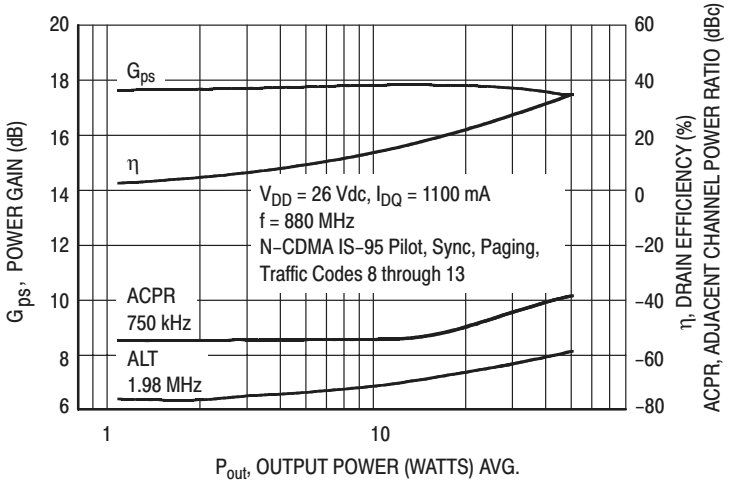



**Figure 9. N–CDMA Performance Output Power versus Gain, ACPR, Efficiency**

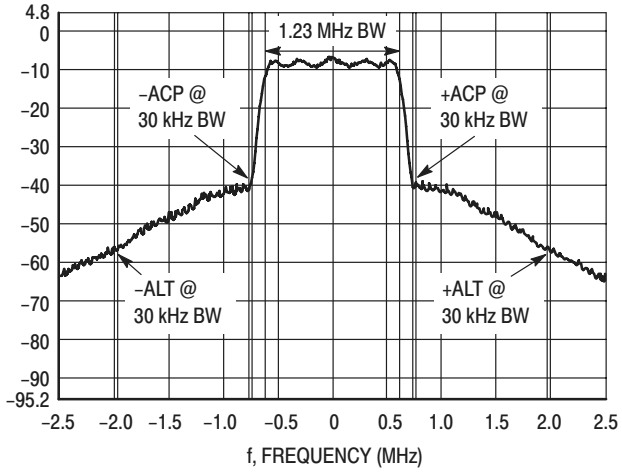
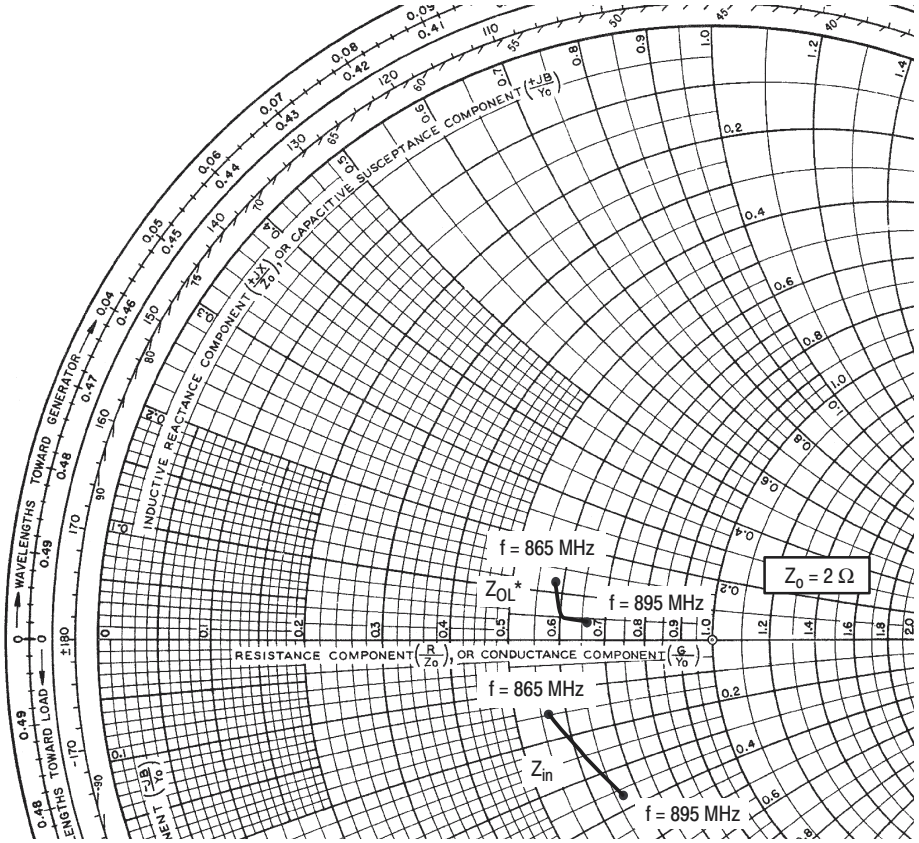



**Figure 10. Typical CDMA Spectrum**




$V_{DD}$ = 26 V, $I_{DQ}$ =1100 mA, $P_{out}$ = 25 W Avg.

| f<br>MHz | $Z_{in}$<br>Ω | $Z_{OL}$*<br>Ω |
|---|---|---|
| 865 | 1.15 – j0.3 | 1.17 + j0.24 |
| 880 | 1.25 – j0.5 | 1.22 + j0.1 |
| 895 | 1.35 – j0.75 | 1.32 + j0.07 |

$Z_{in}$ = Complex conjugate of source impedance.

$Z_{OL}$* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: $Z_{OL}$* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

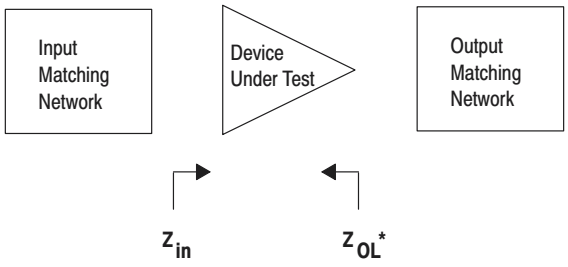


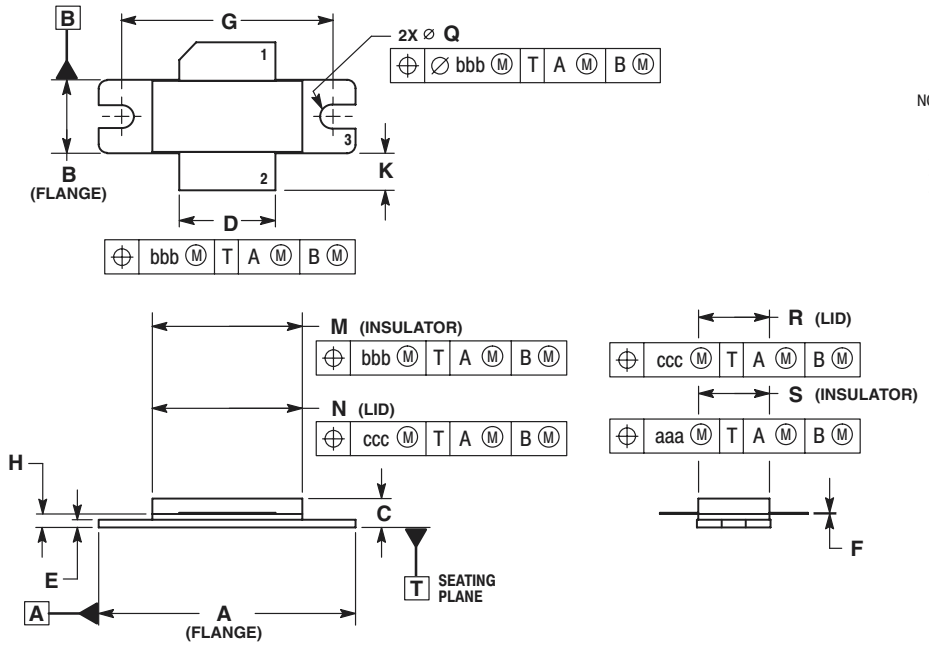

**Figure 11. Series Equivalent Input and Output Impedance**

# NOTES

# NOTES

# NOTES

## PACKAGE DIMENSIONS

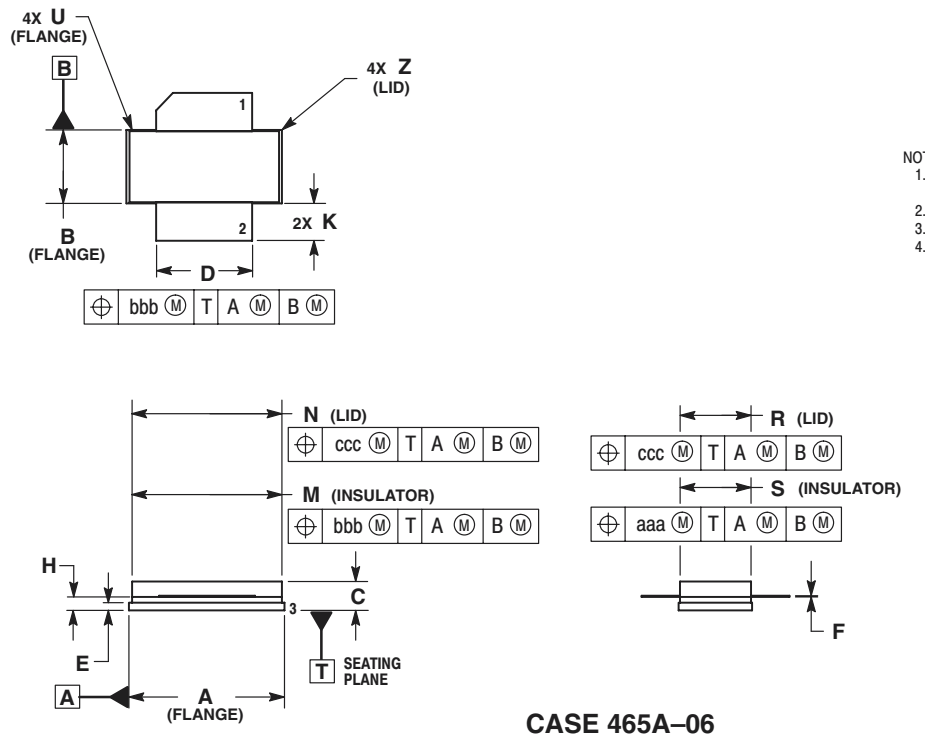



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.335 | 1.345 | 33.91 | 34.16 |
| B | 0.380 | 0.390 | 9.65 | 9.91 |
| C | 0.125 | 0.170 | 3.18 | 4.32 |
| D | 0.495 | 0.505 | 12.57 | 12.83 |
| E | 0.035 | 0.045 | 0.89 | 1.14 |
| F | 0.003 | 0.006 | 0.08 | 0.15 |
| G | 1.100 BSC | | 27.94 BSC | |
| H | 0.057 | 0.067 | 1.45 | 1.70 |
| K | 0.170 | 0.210 | 4.32 | 5.33 |
| M | 0.774 | 0.786 | 19.66 | 19.96 |
| N | 0.772 | 0.788 | 19.60 | 20.00 |
| Q | ∅.118 | ∅.138 | ∅3.00 | ∅3.51 |
| R | 0.365 | 0.375 | 9.27 | 9.53 |
| S | 0.365 | 0.375 | 9.27 | 9.52 |
| aaa | 0.005 REF | | 0.127 REF | |
| bbb | 0.010 REF | | 0.254 REF | |
| ccc | 0.015 REF | | 0.381 REF | |

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

**CASE 465–06**
**ISSUE F**
**NI–780**
**MRF9135L**

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| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.805 | 0.815 | 20.45 | 20.70 |
| B | 0.380 | 0.390 | 9.65 | 9.91 |
| C | 0.125 | 0.170 | 3.18 | 4.32 |
| D | 0.495 | 0.505 | 12.57 | 12.83 |
| E | 0.035 | 0.045 | 0.89 | 1.14 |
| F | 0.003 | 0.006 | 0.08 | 0.15 |
| H | 0.057 | 0.067 | 1.45 | 1.70 |
| K | 0.170 | 0.210 | 4.32 | 5.33 |
| M | 0.774 | 0.786 | 19.61 | 20.02 |
| N | 0.772 | 0.788 | 19.61 | 20.02 |
| R | 0.365 | 0.375 | 9.27 | 9.53 |
| S | 0.365 | 0.375 | 9.27 | 9.52 |
| U | --- | 0.040 | --- | 1.02 |
| Z | --- | 0.030 | --- | 0.76 |
| aaa | 0.005 REF | | 0.127 REF | |
| bbb | 0.010 REF | | 0.254 REF | |
| ccc | 0.015 REF | | 0.381 REF | |

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

**CASE 465A–06**
**ISSUE F**
**NI–780S**
**MRF9135LSR3**

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